

# PHILCO

## TRANSISTOR GUIDE FOR SWITCHING CIRCUIT DESIGNERS

(Application Lab Report 691)

*Covering  
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of Switching  
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*ION LAB REPORT 691*

## Transistor Guide For Switching Circuit Designers

By J. Hildebeitel and P. Thomas

The design engineer is often faced with the problem of selecting the proper transistor for his particular application. In the field of "switching" there are various circuits which are used as basic building blocks; these building blocks are then interconnected in some fashion to form the overall system, perhaps a computer. In this paper we shall consider two of the most commonly used building blocks; namely, the inverter and the flip-flop. The following is mainly a discussion of the pertinent properties of the transistor which are needed to obtain the optimum performance of these two building blocks in different types of "transistor logic". A discussion of the inverter and the flip-flop are certainly related since the flip-flop is nothing more than the interconnection of two inverters.

From a circuit viewpoint, different types of transistor logic are formed essentially by changing the coupling element between transistors. Coupling elements such as direct connections, resistors, diodes, and resistor capacitor combinations are most common. Let us discuss the two basic building blocks for various types of transistor logic and thus derive the desirable qualities of the transistor for these applications.

Certainly the simplest coupling element between transistors is a direct connection. The logic thus formed is termed "Direct Coupled Transistor Logic" (DCTL).

### DCTL

The basic inverter and flip-flop are shown in Figures 1 and 2.

DCTL is one of the many types of saturated transistor logic; i.e., when the transistor is ON it is saturated and thus the voltage from collector to emitter is very small (.05V to 0.15V). With reference to Figure 1, consider the case where all of the input transistors are ON; then their output voltage ( $V_{sat}$ ) will be applied to the next transistor. The base voltage needed to turn a tran-

sistor ON is approximately 0.25 to 0.4 volts, therefore the middle transistor will be OFF. Since this middle transistor is OFF its collector current will be small and the collector to emitter voltage will try to take on the value  $-V_{CC}$ . This action will turn the output stages ON, however, the forward biased base-emitter diodes of the output stages will clamp the collector voltage of the middle stage to  $V_{BEon}$  of the output transistors. It is seen that the collector voltage swing of any given stage is from  $V_{sat}$  to  $V_{BEon}$ . A typical transistor input characteristic is shown in Figure 3. Notice that the transistor is never really OFF; i.e., some small base current flows even in the OFF state.

Notice also that the ON base current is different for variations in input characteristics of the output transistors. The lack of unique ON and OFF states, where the OFF base current is dependent upon  $V_{sat}$  and the ON base current is dependent upon  $V_{BEon}$ , places severe requirements upon the transistor. Let us discuss the importance of the various DC transistor parameters in this type of logic.

A low saturation voltage ( $V_{sat}$ ) is desirable, for this limits the current in the OFF state. It is this parameter which determines the maximum number of fan ins. From the above discussion of Figure 3, one realizes the necessity for transistors with small variations in  $V_{BEon}$ . It is this parameter which has the most effect in determining the maximum number of fan outs. Also notice that since  $V_{BEon}$  decreases with increasing temperature, the output voltage swing will do likewise.

A transistor with moderately high DC current gain,  $h_{FE}$ , is desirable so as to insure saturation of the transistor which receives the lowest base current (transistor  $T_1$  in Figure 3). Of course, a tight specification on the variation of  $V_{BEon}$  will lessen the need for a high  $h_{FE}$ .

A transistor with low  $I_{CBO}$  is required for DCTL.

**PIONEER IN THE DEVELOPMENT AND MANUFACTURE OF SEMICONDUCTOR DEVICES**

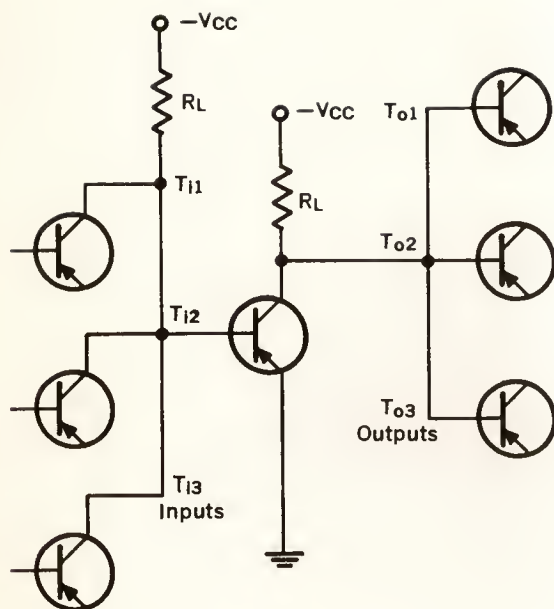


FIGURE 1—DCTL INVERTER

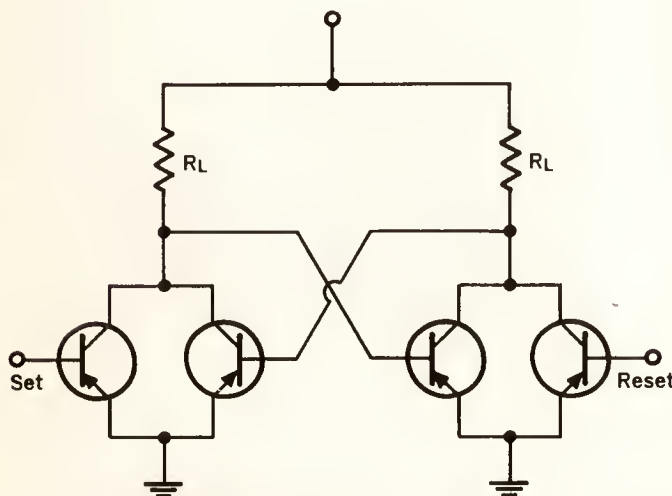


FIGURE 2—DCTL FLIP-FLOP

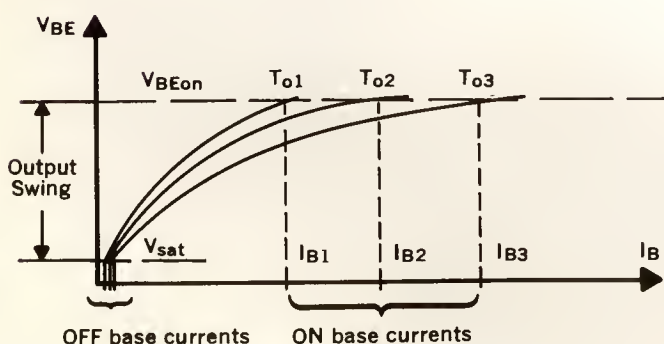


FIGURE 3—INPUT CHARACTERISTIC

This is so because the collector current due to  $I_{CBO}$  is multiplied by some fraction of  $h_{FE}$ . Since  $I_{CBO}$  increases exponentially with temperature and since the switched collector current normally employed in DCTL is low, a condition may be reached where the transistor collector voltage will be held at a low value because of the fractional  $h_{FE}I_{CBO}R_L$  drop. It is interesting to note that the temperature variation of  $I_{CBO}$  and  $V_{BEon}$  limits the reliable operating range of DCTL to 55°C.

To summarize, a transistor to be used in DCTL should possess the following DC qualities: a low maximum  $V_{sat}$ , a high minimum  $V_{BE}$  with a very narrow spread in this parameter, a moderately high  $h_{FE}$ , and a low  $I_{CBO}$ . Because of the small voltage swings involved, breakdown voltage ratings have very little importance in DCTL.

Since switching speed is an important consideration in most applications, a discussion of the relative importance of the transistor transient response parameters in DCTL is in order.

In most cases the ON base current of the transistor is large; i.e., the transistor is driven hard into saturation. Thus one would expect short rise-times. Likewise, since the overdrive base current is large and since no turn-off current is supplied, one would expect long hole storage-times and moderate fall-times. Also, as a consequence of not having a turn-off current, turn-on delay-times are quite small. From this, one may well conclude that the transient response parameter of greatest importance is the hole storage factor ( $K'_s$ ); this should be low as possible.

The severe disadvantages of DCTL; i.e., small output voltage swing, limited temperature, and lack of turn-off current, lead one to search for coupling schemes other than direct connection. One possible scheme which overcomes the above mentioned disadvantages is the use of coupling diodes. One such popular silicon diode is called the Stabistor and thus the name "Stabistor Coupled Transistor Logic" (SCTL).

### SCTL

The basic inverter and flip-flop building blocks for SCTL are shown below in Figures 4 and 5.

Note the two main changes in the basic building blocks. First is the insertion of a silicon diode which increases the output voltage swing from  $(V_{BEon} - V_{sat})$  to  $(V_{BEon} + V_D) - V_{sat}$ . Thus the voltage swing increases from approximately 0.3 V in DCTL to 1.0 V in SCTL. Secondly, a turn-off current is supplied by  $V_{BB}$  thru  $R_{BB}$ . This reduces the hole storage- and fall-times and insures a definite OFF state.

Let us again consider the DC and transient parameters of the transistor separately.

The addition of the silicon diode greatly reduces the restriction on the saturation voltage ( $V_{sat}$ ). This is true because the saturation voltage must become larger than the initiation voltage of the silicon diode before it can

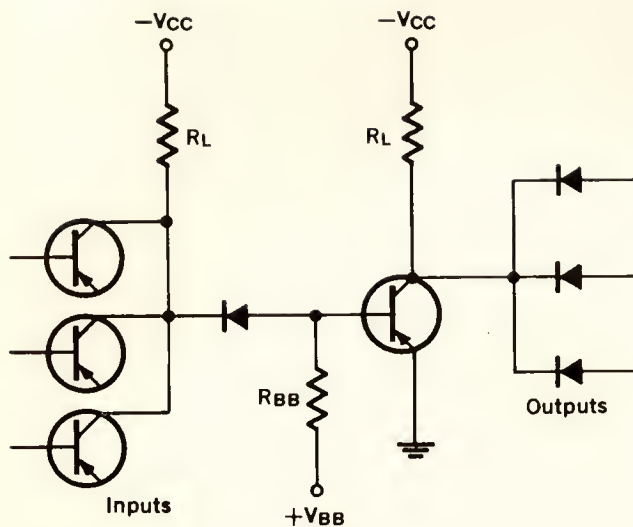


FIGURE 4—SCTL INVERTER

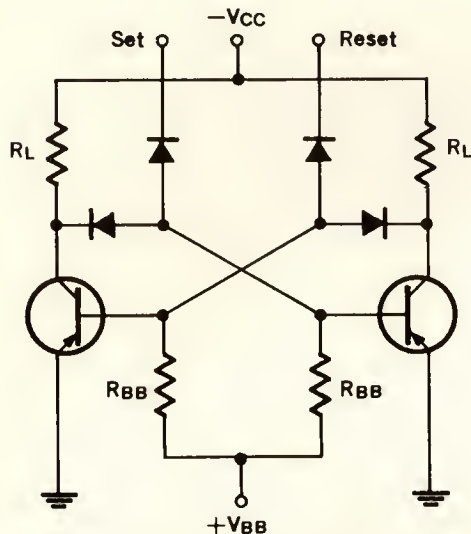


FIGURE 5—SCTL FLIP-FLOP

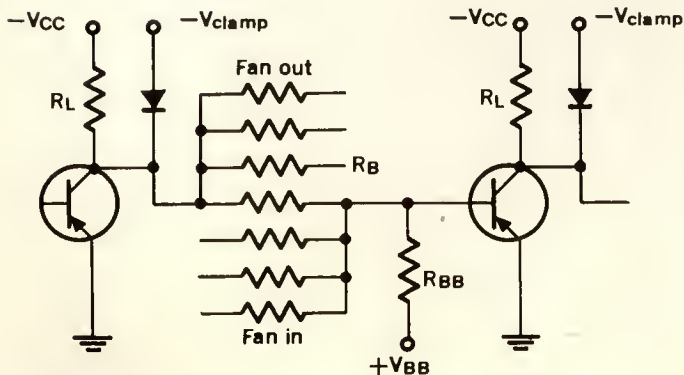


FIGURE 6—RTL INVERTER

influence the following stage. This greatly increases the number of possible inputs over DCTL. The considerations of DCTL for  $V_{BEon}$  and  $h_{FE}$  still hold for SCTL, for the problem of base current division between output stages still exists. In fact, this problem can become more severe than in DCTL if diode variations are not kept to a minimum. In SCTL, since a turn-off bias is employed,  $I_{CBO}$  does not get multiplied by any fraction of  $h_{FE}$ . Thus the collector current in the OFF state is just  $I_{CBO}$ , therefore, this parameter is less important in SCTL than in DCTL.

To summarize, a transistor to be used in SCTL should possess the following DC qualities: a narrow spread in  $V_{BEon}$ , a moderately high  $h_{FE}$  and a moderately low  $I_{CBO}$ . Again, because of the small voltage swings involved, the collector voltage rating is of no importance. However, since a turn-off circuit is employed, one must consider the emitter-base breakdown rating if diffused-base transistors are employed.

Since a turn-off current is employed in SCTL, hole storage- and fall-times may be reduced over those found in DCTL. Although the hole storage factor ( $K'_s$ ) is still important, it is no longer the limiting factor in determining the transient response. While the use of a turn-off current reduces the turn-off times, its use leads to an increase in turn-on delay-time. This is because the base-emitter diode is reversed biased in the OFF state and the turn-on delay-time charge ( $Q_{off}$ ) is a function of this reverse bias. Therefore turn-on delay-time charge,  $Q_{off}$ , is an important consideration as well as the rise, fall, and storage time constants,  $T_{RE}$ ,  $T_{FE}$ , and  $K'_s$ .

\* Replacement of the diode used in SCTL with a resistor gives rise to Resistor Transistor Logic (RTL).

### RTL

The resistor is less expensive than the diode and it permits greater signal swings. The increase in signal swing has two advantages; namely, greater fan-in and fan-out are permitted and noise immunity is enhanced. The basic building blocks (inverter and the flip-flop) are shown below in Figures 6 and 7.

If power supplies are not a major consideration, one may increase the value of  $V_{CC}$  and  $R_L$  (keeping the switched collector current constant) and clamp the collector to some arbitrary level. In this way the number of fan outs and fan ins may be greatly increased.

The inverter may be in one of two states. These states are as follows: the collector is at  $V_{sat}$  (ON) when at least one of the fan in collectors is at  $V_{CC}$  or  $V_{clamp}$ ; the collector is at  $V_{CC}$  or  $V_{clamp}$  (OFF) when all of the fan in collectors are at  $V_{sat}$ . Since the inverter is an "and gate" for near zero signals and an "or gate" for negative signals, two types of gate function are possible depending upon the choice of the "true" signal.

Due to the increase in signal swing, a higher voltage rating is required of transistors in RTL than in any

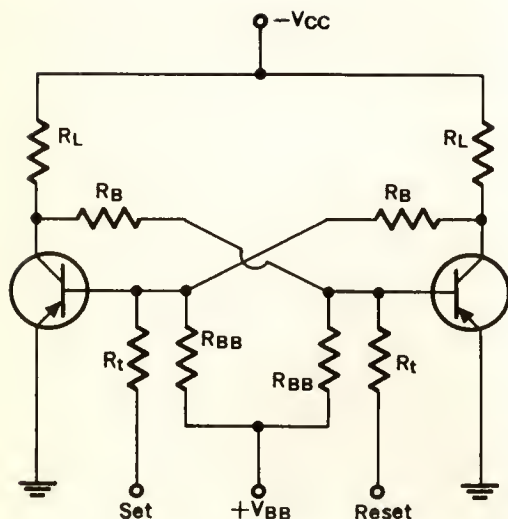


FIGURE 7—RTL FLIP-FLOP

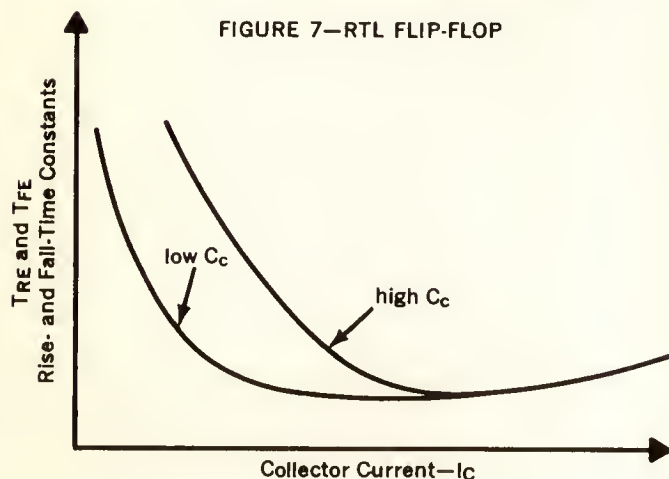


FIGURE 8— $T_{RE}$ ,  $T_{FE}$  VERSUS  $I_{CS}$

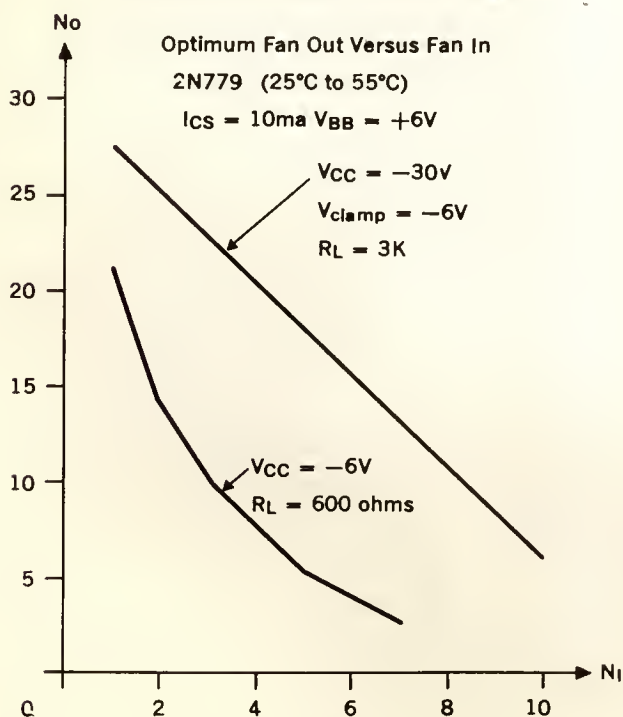


FIGURE 9

of the above mentioned logics. Collector voltages of 5V to 12V and switched collector currents of 3 ma to 30 ma are common. Since a turn-off current is provided, any limitations imposed by the reverse breakdown voltage of the base-emitter diode must be observed. A high  $h_{FE}$  (greater than 40) is desired for fan in and fan out reasons, as is a low  $I_{CBO}$ . A high minimum  $V_{BEon}$  and a low maximum  $V_{sat}$  are important; however, equally important is the specification spread (max to min) of these two parameters. A tight  $V_{sat}$  and  $V_{BEon}$  spec is most desirable of an RTL transistor if high fan in and fan out are to be obtained. The Precision-Etch\* process of transistor production, with its resulting parameter uniformity, lends itself to this need for tight specifications.

The choice of switched collector current may be partially dictated by transient response considerations. For example, the rise- and fall-time constants,  $T_{RE}$  and  $T_{FE}$ , exhibit a minimum over some finite range of collector current. This is shown in Figure 8.

Note that a low collector capacity is desirable to prevent the current, at which  $T_{RE}$  and  $T_{FE}$  exhibit their minimum, from becoming prohibitively large. It is worth mentioning that since the signal swings in RTL are large, the gain bandwidth product,  $f_T$ , should be relatively constant over the range of this swing.

Rise-times in RTL are long, the worst case occurring when one inverter turns ON all of its fan outs; thus a low  $T_{RE}$  is desirable. Fall- and storage-times are long because the available turn-off current is small. The worst case for storage time occurs when an inverter is turned ON by all of its fan ins. In this case, the excess base current is largest. Thus one desires a low  $K'_s$  and  $T_{FE}$ . The turn-off circuit is designed for worst case: end-of-life and high temperature. If a condition other than this prevails, the turn-off will be over-compensated and the base-emitter diode will take on a reverse voltage. This may lead to appreciable turn-on delay time and so a low  $Q_{off}$  is desirable. As one may conclude from the above discussion, RTL is inherently a slow logic (presently <20 mc).

The Philco 2N779 Micro Alloy Diffused-base Transistor (MADT\*\*) is an excellent transistor for use in RTL; its specification is formed around the qualities dictated by this type of logic. Figure 9 shows curves of maximum fan out versus fan in for this transistor. Worst case design for a temperature range of 25°C to 55°C was used. Two curves are given: one curve is for a -6 volt collector supply, 10 ma collector current, and 6V turn-off; the other is for a -6 volt clamped collector, -30V collector supply, 10 ma current, and 6V turn-off. These curves represent fan out and fan in obtainable when optimum values of coupling and turn-off resistors are used. When available resistance values (5%) are used, these curves shift downward somewhat. This effect is noted in Table I, where resistance values

\*Trademark Philco Corp.

\*\*Reg. U.S. Pat. Off.

# PHILCO SWITCHING

Frequency of Operation (Rep Rate)	Saturated RTL Low-Level Circuits		Saturated RCTL Low-Level Circuits		Saturated DTL Low-Level Circuits	
	Ge	Si	Ge	Si	Ge	Si
0-10 KC	2N224 2N1129 2N1130		2N226 2N1129 2N1130		2N226 2N1129 2N1130	
10-50 KC	2N597 2N1123 2N1478	2N496	2N224 2N536 2N1125	2N496	2N224 2N536 2N1125	2N496
50-200 KC	2N598 2N599	2N1428 2N1429	2N597 2N598 2N1123 2N1478	2N496 2N1119 2N1428 2N1429	2N597 2N598 2N1123 2N1478	2N496 2N1119 2N1428 2N1429
.2-1 MC	2N393 2N1122 2N1122A 2N1427 2N1499A	2N1663	2N393 2N599 2N1122 2N1122A 2N1427 2N1499A	2N496 2N1119 2N1428 2N1429	2N393 2N599 2N1122 2N1122A 2N1427 2N1499A	2N496 2N1119 2N1428 2N1429
1-5 MC	2N501 2N501A 2N768 2N779 2N1500	2N1663	2N393 2N768 2N1122A 2N1427	2N1199 2N1199A 2N1472 2N1663	2N393 2N768 2N1122 2N1122A 2N1427	2N1199 2N1199A 2N1472 2N1663
5-20 MC	2N769 2N779		2N501A 2N768 2N779 2N1500	2N1472 2N1663	2N501A 2N768 2N779 2N1500	2N1472 2N1663
20-50 MC			2N769 2N779		2N769 2N779	
50-300 MC			2N769		2N769	

# NG TRANSISTORS

DCTL Low-Level Circuits		Non-Saturating Low-Level Current Switching Circuits		Medium-Level Switching Circuits (up to 400 ma)		High-Level Switching Circuits DC-to-DC Converters Static Relays	
Ge	Si	Ge	Si	Ge	Si	Ge	Si
2N224 2N1129 2N1130				2N223 2N224 2N226 2N1124		2N386 2N387	
2N536	2N496			2N1125 2N1130		2N670 2N671	
2N240	2N496 2N1119 2N1428 2N1429			2N600 2N601 2N1123			
2N240 2N393 2N1411	2N496 2N1119 2N1428 2N1429			2N601			
2N393 2N768	2N1199 2N1472 2N1663	2N1204 2N1494		2N1204 2N1494			
2N501A 2N768 2N1500		2N1204 2N1494		2N1204 2N1494			
		2N1204 2N1494		2N1204 2N1494			
		2N769					

Table I—Discrete Fan Out and Fan In

No	N <sub>I</sub>	R <sub>L</sub>	R <sub>B</sub>	R <sub>BB</sub>	V <sub>CC</sub>	V <sub>clamp</sub>
6	10	3K	4.3K	10K	-30	-6
10	8	3K	6.8K	18K	-30	-6
16	5	3K	12K	39K	-30	-6
2.5	7	600 ohms	3.6K	12K	-6	X
5	5	600 ohms	4.3K	18K	-6	X
10	3	600 ohms	4.7K	30K	-6	X

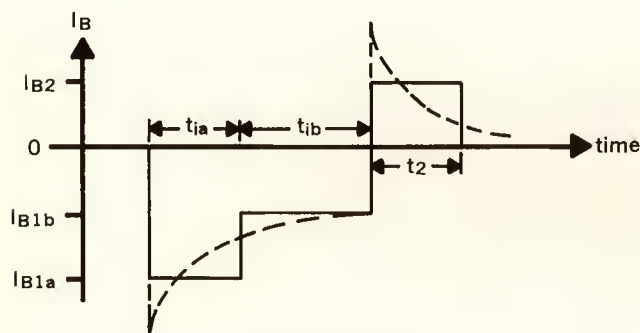


FIGURE 10—BASE CURRENT TRANSIENT

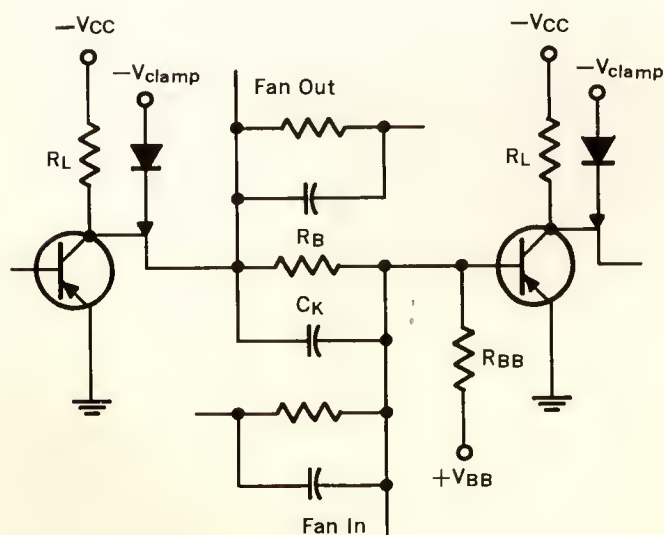


FIGURE 11—INVERTER

are tabulated for three discrete fan out—fan in points. This fan out may be compared to the curve where optimum fan out is given.

Paralleling the resistor of RTL with a speed-up capacitor results in the fastest type of saturated switching logic "Resistor Capacitor Transistor Logic" (RCTL).

### RCTL

The charge stored in the capacitor aids in speeding turn-on and turn-off. Figure 10 gives the ideal base current wave form. The component  $I_{B1a}$  is of sufficient magnitude to provide the desired rise time ( $t_{ia} \approx t_r$ ) and  $I_{B1b}$  holds the transistor to the edge of saturation so that, ideally, there is no hole-storage-time. The current,  $I_{B2}$ , is sufficient to provide the desired fall-time ( $t_2 \approx t_f$ ) and ideally, it ceases to flow when the fall transient is completed. Use of the speed-up capacitor in a practical circuit gives rise to the dotted waveform of Figure 10; this is a good compromise to the ideal waveform. When the transient response constants,  $T_{RE}$ ,  $T_{FE}$ ,  $K'_s$  and  $Q_{off}$ , are known, the size of this capacitor may be calculated as

$$C_K > (K'_s I_{BX} + T_{FE} I_{CS}) / V_{CC}$$

where  $I_{BX}$  is the excess base current.

The basic inverter and flip-flop are shown in Figures 11 and 12. The flip-flop shown employs one possible trigger method, that of using three steering diodes. With this configuration, it is possible to trigger from a sine-wave as well as from a pulse-train.

Essentially the same transistor qualities mentioned for RTL are desirable for RCTL. RCTL is a fast logic, but problems of crosstalk are introduced by the presence of the capacitor. A noise spike may easily propagate throughout the entire system. Peak currents introduced by the capacitor may present a problem.

The Philco 2N769 MADT transistor is ideally suited for very high speed logic. It is at present the world's fastest commercially available switch. Using the circuit of Figure 12, with the values tabulated in Table II, a binary counter was designed capable of operation at 125 mc. Sophisticated circuitry could easily increase the maximum repetition rate of a counter using the 2N769 beyond 125 mc.

In the general discussion of RCTL, it was stated that although this type of logic was a very high speed logic, it also possessed a severe crosstalk problem. The use of diodes will relieve this crosstalk problem. Such a logic configuration is called "Diode Transistor Logic" (DTL).

### DTL

The basic building blocks (inverter and flip-flop) are shown in Figures 13 and 14.

Note the extreme similarity to RCTL, especially in the flip-flop. Because of this similarity, one might expect that the required transistor characteristics are almost identical to those of RCTL. There is one major difference. Notice, in the inverter, that when a stage is

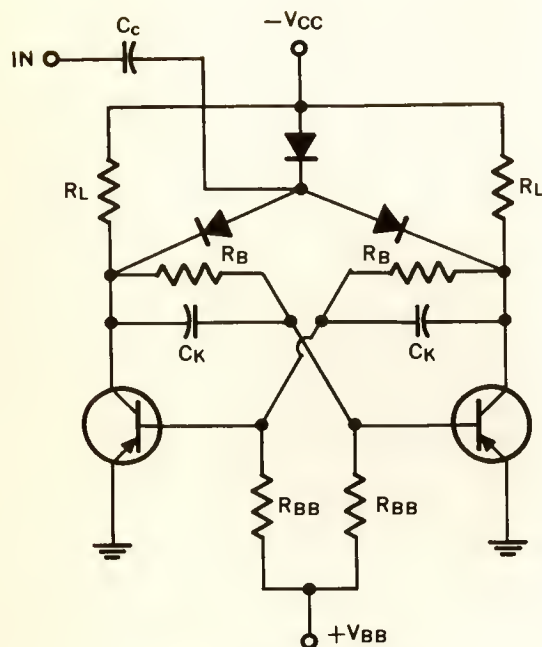


FIGURE 12—FLIP-FLOP

Table II—125 mc Binary Counter Using the 2N769  
Input: 5V p.p. 125 mc Sine Wave

$V_{CC} = -6V$	$R_L = 220 \text{ ohms}$	$C_K = 18 \text{ pf}$
$V_{BB} = +4.5V$	$R_K = 3.3K$	$t_r = 1\text{nsec}$
$C_c = 910 \text{ pf}$	$R_{BB} = 8.2K$	$t_f = 1.5\text{nsec}$

(All diodes Q-6-100)

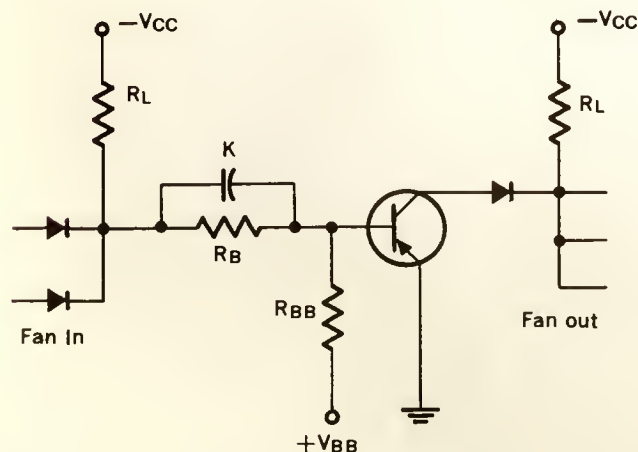


FIGURE 13—INVERTER

saturated and its collector takes on a value  $V_{sat}$ , the following stage sees a voltage equal to  $V_{sat} + V_D$ , where  $V_D$  is the forward drop across the diode. Thus the following stage, which is off, requires a larger turn-off current to be supplied from  $V_{BB}$  and  $R_{BB}$ . This, of course, limits the number of fan ins.

To summarize, the transistor required for DTL is almost identical to that required for RCTL except that the restrictions on magnitude and spread of  $V_{sat}$  are not nearly as important in DTL. It is also worth mentioning that the larger turn-off current in DTL eases the restrictions on the hole storage factor ( $K'_s$ ) and the fall-time factor  $T_{FE}$ .

Non-Saturating Logic may be easily obtained by clamping the transistor out of saturation. A slight increase in speed is obtained but the accompanying increase in power dissipation is an undesirable feature. Thus this type of operation is seldom used.

#### NON-SATURATED LOGIC

Current switching is probably the most popular of the non-saturated switching logics. As a consequence of the non-saturated operation, little turn-on delay-time and no storage-time problems present themselves. The basic building block, shown in Figure 15, is essentially a split-load amplifier with the emitter-follower output driving a common-base stage. This gives rise to complementary outputs. If only an output is needed, the emitter may be clamped to ground as shown in Figure 16.

This very-fast logic involves a signal swing about an operating point rather than ON and OFF switching. Therefore, no large signal parameter linearity is needed. Since the input and output signal are centered about different DC levels, a level shifting device is needed between stages if identical current switches are to be cascaded. The alternate solution, not easily realizable, is to cascade PNP and NPN stages whereby each input operates at the level of the preceding output.

The major requirement of a transistor to be used in current switching is power dissipation. Large power dissipations present a reliability problem as these two are related. Notice also that the power dissipation of circuit components is high.

Because of the low base-impedance of the two stages, a low base spreading resistance,  $r_b'$ , is desirable.  $V_{BEon}$  is relatively unimportant and  $V_{sat}$  is of no interest;  $h_{FE}$  need only be moderate and  $I_{CO}$  is of little interest.

The operating point is usually chosen at the point of highest  $f_T$ , thus insuring small rise and fall times. Rise-time is proportional to the magnitude of the input voltage although there is a limit upon this imposed by the swing of previous stages. It is sometimes advantageous to use an amplifier type transistor in this application (amplifier transistors usually have lower  $r_b'$  than switching type transistors).

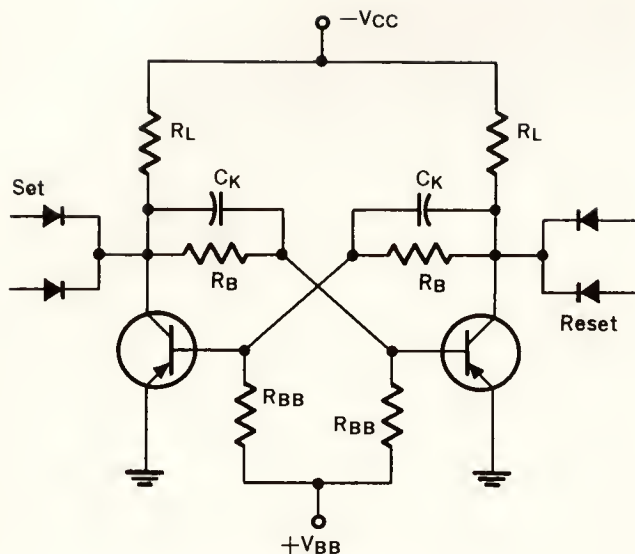


FIGURE 14—FLIP-FLOP

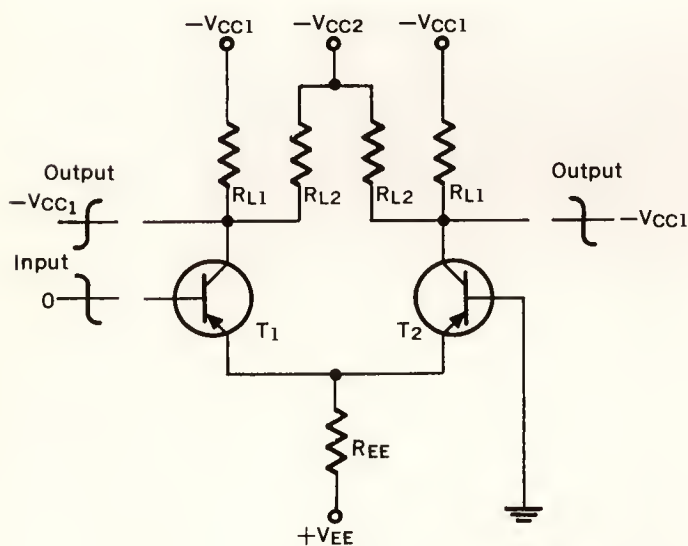


FIGURE 15

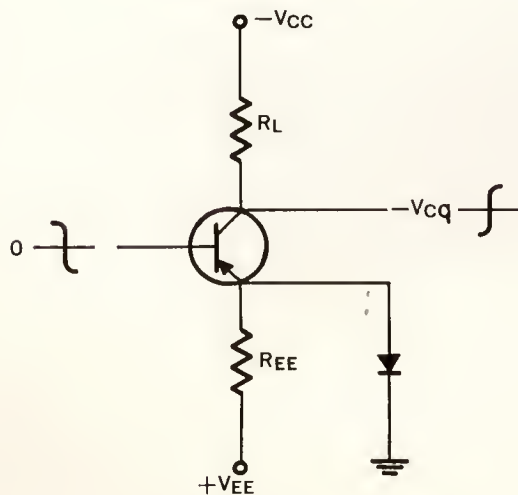


FIGURE 16

Table III gives the circuit values for a current switch using the Philco 2N1204. Also included are the response times as measured at both outputs.

In the foregoing we have discussed different transistors according to their speed and application in different types of logic. Within these categories there often exists the consideration of power. That is, there are some miscellaneous applications where the salient requirement is that the transistor be capable of switching large currents and voltages. We can divide these applications into two categories, namely, those where speed is a consideration, and those where it is not. We shall refer to the first group as medium power (under 1 watt) and the second as high power (over 1 watt).

Table III—Current Switch Using the 2N1204 MADT

$R_{L1} = 180 \text{ ohms}$	$V_{CC1} = -4.5V$	$I_E = 15 \text{ ma}$
$R_{L2} = 1.8K$	$V_{CC2} = -9V$	$V_{in} = 0 \pm 0.5V$
$R_{EE} = 4.7K$	$V_{EE} = +70V$	$V_{out} = -4.5 \pm 0.5V$
$T_1$	$t_r = 12 \text{ nsec}$	$t_f = 8 \text{ nsec}$
$T_2$	$t_r = 7 \text{ nsec}$	$t_f = 12 \text{ nsec}$

#### MEDIUM POWER (Medium High Speed)

In this category we find many of the miscellaneous circuits of a computer such as line drivers, memory-core drivers, power gates, pulse amplifiers, etc. In all of these circuits the switched current is in the general vicinity of 250 ma. It is then obvious that transistors for such applications must have desirable qualities at high collector currents; for example,  $h_{FE}$ ,  $V_{sat}$ ,  $V_{BE}$  and  $T_{RE}$  must show no abnormalities at high collector currents. Of these,  $V_{sat}$  is perhaps the most important for the power dissipation of the transistor in a saturated circuit is  $P_D = I_C \times V_{sat} = (I_C)^2 R_{sat}$ . Substitution of typical values shows that the power dissipation may easily approach 150 mw.

The 2N1204, which is a high-speed, medium-power transistor, is shown in Figure 17, in a line driver circuit.

#### HIGH POWER (Low Speed)

Some applications, such as power converters, relay drivers, servo motor drivers, power supply regulators, etc., require a high-power transistor but speed is of little or no interest. In such applications, the main requirement is the control of large currents at large voltage levels. The Philco 2N386, which possesses these requirements, is shown in Figure 18, in a typical power converter circuit.

In the foregoing discussions, certain aspects of parameter variations have been given little attention; namely, parameter variations due to temperature and aging. Such changes must be dealt with in worst case design. Some parameters are more susceptible to change due to temperature and aging than others.

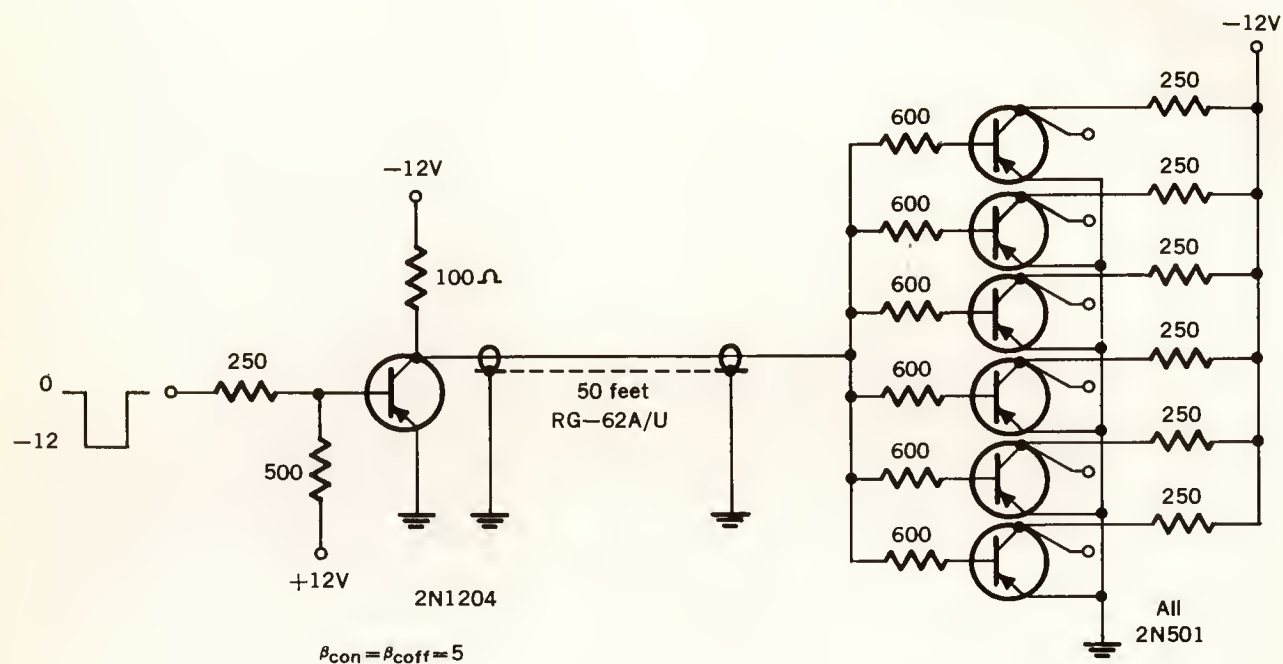
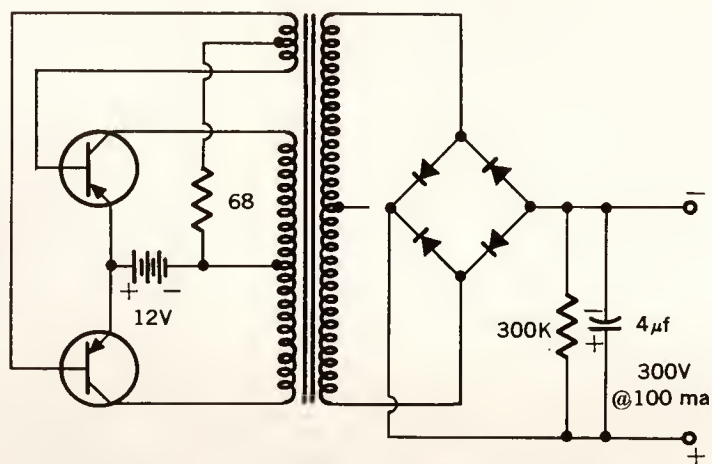


FIGURE 17—2N1204 LINE DRIVER—DRIVING SIX 2N501 INVERTERS



Transformer-Triad TY-695 diodes-Sarkes Tarzian M506

FIGURE 18—2N386 POWER CONVERTER

The information, diagrams, or any other data included herein is believed to be accurate and reliable. However, the Philco Corporation, Lansdale Division assumes no responsibility or liability whatsoever for the application, interpretation, or use made of such information, diagrams, or data especially insofar as the use of said information, diagrams, or data affects any patent, trademark, or proprietary data rights.

## PARAMETER VARIATIONS FOR WORST CASE DESIGN

There are many opinions as to what "rules-of-thumb" should be used in worst case design. The following are given only as a guide for most general cases and should not be considered mandatory for such design. Let us consider parameter variations with temperature and aging separately.

### Temperature—

The largest variations with temperature seem to exist for  $I_{CBO}$  which is an exponential function of temperature.  $I_{CBO}$  approximately doubles for every  $10^{\circ}\text{C}$  rise in junction temperature.

$V_{BEon}$  is found to decrease with temperature at a rate of approximately 2 mv per  $^{\circ}\text{C}$  rise in junction temperature.

DC current gain,  $h_{FE}$ , is lowest at low temperatures, decreasing approximately 30% for junction temperature variations from  $+25^{\circ}\text{C}$  to  $-25^{\circ}\text{C}$ .

Saturation voltage increases slightly with temperature. The variation is usually less than 20% for junction temperature variations from  $+25^{\circ}\text{C}$  to  $+65^{\circ}\text{C}$ .

For most alloy type transistors, such as alloy junction, Surface Barrier, Micro Alloy Transistor, and Micro Alloy Diffused-base Transistors, variations in  $T_{RE}$ ,  $T_{FE}$ , and  $Q_{off}$  are so small that they are usually neglected. Of the four transient response parameters,  $K'_s$  is the most temperature dependent. The increase in  $K'_s$  is usually less than 30% for an increase in junction temperature from  $25^{\circ}\text{C}$  to  $55^{\circ}\text{C}$ .

### Aging—

Here, of course, the degradation in parameter performance is dependent upon the length of aging. Therefore it is only right to mention which parameters will show the greatest degradation at end of life.  $V_{sat}$  and  $V_{BEon}$  are found to be very stable with life and are usually derated by no more than 10%.  $h_{FE}$  and  $I_{CBO}$  are found to be less stable with life and are usually derated by approximately 20% and 100%, respectively, depending upon the unit.

Variations in transient response parameters with life are usually neglected because of the small changes involved.

From the foregoing discussion, it is apparent that it is necessary to incorporate these transistor parameter variations into the circuit design.

## LIST OF DEFINITIONS USED IN THIS BROCHURE

$h_{FE}$	The DC current gain of the transistor in the common emitter connection.
$V_{sat}$	The voltage appearing from collector-to-emitter of the transistor when the transistor is operated in the saturated region.
$V_{BEon}$	The voltage which appears from base-to-emitter when transistor is operated in the saturated region.
$I_{CBO}-I_{CO}$	The collector cutoff current of the transistor.
$r_b'$	Base spreading resistance.
$C_{TC}$	Collector barrier capacity. This capacity greatly influences the rise- and fall-times when switching low collector currents.
$C_{TE}$	The emitter barrier capacity. This capacity is most influential in determining the turn-on delay time.
$T_{RE}$	Rise-time constant. This constant is used in determining the rise-time of a basic inverter circuit.
$T_{FE}$	Fall-time constant. This constant is used in determining the fall-time of a basic inverter circuit.
$K'_s$	Hole storage factor. This quantity is used in determining the hole storage time in an inverter circuit.
$Q_{off}$	Turn-on delay-time charge. This quantity represents the charge on the transistor when the transistor is in the OFF state. The time required to remove this charge represents the turn-on delay-time.
$f_T$	The current gain-bandwidth product of the transistor.
$\beta_c (ON)$	The ratio of the switched collector current to the ON base current.
$\beta_c (OFF)$	The ratio of the switched collector current to the OFF base current.
$I_{BX}$	Excess base current. The base current in excess of that just needed to saturate the transistor.
$V_{CC}$	Collector supply voltage.
$V_{BB}$	Turn-off base current supply voltage.
$V_I$	Voltage dropped across a forward biased diode.

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